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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/847,163	05/01/2001	Tatsuru Namatame	15.43/5851	5642

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EXAMINER	
FOONG, SUK SAN	
ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 08/14/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/847,163	Applicant(s) NAMATAME ET AL.	
	Examiner Suk-San Foong	Art Unit 2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 6-16 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 6-15 is/are rejected.

7)☒ Claim(s) 16 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Applicant's election of Group II, claims 6-16, in Paper No. 9 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 14 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 14, line 3, it is questioned what is recited through "60 degrees or greater less than 90 degrees".

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 6-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maruo ('090) in combination with Tanaka ('577).

Maruo teaches a method of forming high breakdown voltage CMOS transistors which includes forming silicon oxide film 14' over substrate 10 (Col. 7, line 60-62, and Fig. 3B), then forming silicon nitride film over substrate 10 (Col. 7, lines 63-64), etching silicon nitride film 26 to expose portions of substrate 10 that are not in element forming regions (Col. 7, lines 64-65, and Fig. 3C), then applying photoresist 27 over substrate 10 and providing openings at LOCOS forming regions (Col. 7, line 66 to Col. 8, line 1), subsequently implanting impurity at openings of first and second LOCOS regions 17 (Col. 8, lines 1-6, and Fig. 3C), then applying and patterning photoresist 27 to form channel stopper regions 12 (Col. 8, lines 7-15, and Fig. 3D), then performing wet oxidation at 950°C to form LOCOS oxide layers 11 and 15 such that first and second offset impurity layers are below LOCOS layers 15 (Col. 8, lines 16-20, and Fig. 3E), then growing gate dielectric layer 14'' after removing silicon nitride layer 26 and oxide layer 14' from substrate 10 (Col. 8, lines 23-27, and Fig. 3F), subsequently forming gate electrodes 16 and

20 in between LOCOS oxide layers 11 and 15 (Col. 8, lines 38-44, and Fig. 3F), and then forming source and drain regions 18 and 18a such that first LOCOS oxide layer 15 is between gate dielectric layer 14'' and drain region 18, and second LOCOS oxide layer is between gate dielectric layer 14'' and source region 18a (Col. 9, lines 11-16, and Fig. 3I).

Maruo does not teach forming first and second recessed sections where LOCOS layers are to be formed.

Tanaka teaches a method of manufacturing semiconductor device with which includes providing semiconductor substrate 1, then forming oxide layer 2 and nitride layer or anti-oxidation 3 over substrate 1 (Col. 2, lines 59-60, and Fig. 2A), then patterning oxide layer 2 and anti-oxidation layer 3 through photoresist 5 (Col. 3, lines 57-59), subsequently forming first and second recessed sections in regions where first and second semi-recessed LOCOS are to be formed by etching substrate 1 (Col. 3, lines 60-62), then implanting impurity in regions where substrate 1 is exposed such as first and second recessed sections (Col. 3, lines 62-65, and Fig. 2B), subsequently removing photoresist 5 (Col. 3, lines 66), then thermally oxidizing substrate 1 to form oxide films 7 on offset impurity layers 6 by using anti-oxidation layer 3 as mask (Col. 3, line 67 to Col. 4, line 4), subsequently removing anti-oxidation layer 3 and oxide layer 2 (Col. 4, lines 6-7), and forming gate oxide film 9 (Col. 4, line 8, and Fig. 1D).

It would have been within the scope to one ordinary skill in the art to combine both teachings because it would enable the formation of LOCOS oxide layers 11 and 15 of Maruo to be performed and obtain further advantage of decreasing parasitic capacitance with respect to the gate electrode (Tanaka, Col. 4, lines 17-18).

With respect to claim 8, the choice of thickness of anti-oxidation layer would have been a matter of routine optimization to achieve the desired device densities and the desired device characteristics to be formed. (See MPEP 2144.05)

7. Claims 9-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maruo in combination with Tanaka as applied to claims 6-8 above, and further in view of Luning et al. ('963).

The combination of Maruo and Tanaka do not teach formation of protection film prior to implanting impurity.

Luning et al. disclose formation of protective or screen oxide layer over exposed portions of substrate (Col. 3. lines 65-67), then implanting ions through screen oxide layer (Col. 4, lines 1-3), subsequently removing screen oxide layer from substrate (Col. 4, lines 5-7), and forming gate oxide layer.

It would have been within the scope to one ordinary skill in the art to combine the teachings of Luning et al. with combination of Maruo and Tanaka because it would enable formation of protective film layer over semiconductor substrate and in first and second recessed sections of Maruo and Tanaka to be performed and obtain further advantage of preventing contamination by other impurities during implant.

8. Claims 13-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maruo in combination with Tanaka as applied to claims 6-8 above.

Claims 13 and 14 are opened to forming recessed sections with tapered configuration with an angle that deviates from normal line and, claim 15 is also open to implanting at an angle that deviates from the normal line to an extent which would not be expected to substantially alter the process of the reference. For example, an implantation angle which differs 0.01° from normal line would be expected to produce a doping profile first and second recessed sections that is essentially the same as the doping profile resulting from the disclosed the normal line implant.

Allowable Subject Matter

9. Claim 16 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suk-San Foong whose telephone number is 703-305-0383. The examiner can normally be reached on Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 703-308-4918. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 (7724, 3431, 3432).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

SF
August 10, 2002

George Fourson
Primary Examiner
Art Unit 2823